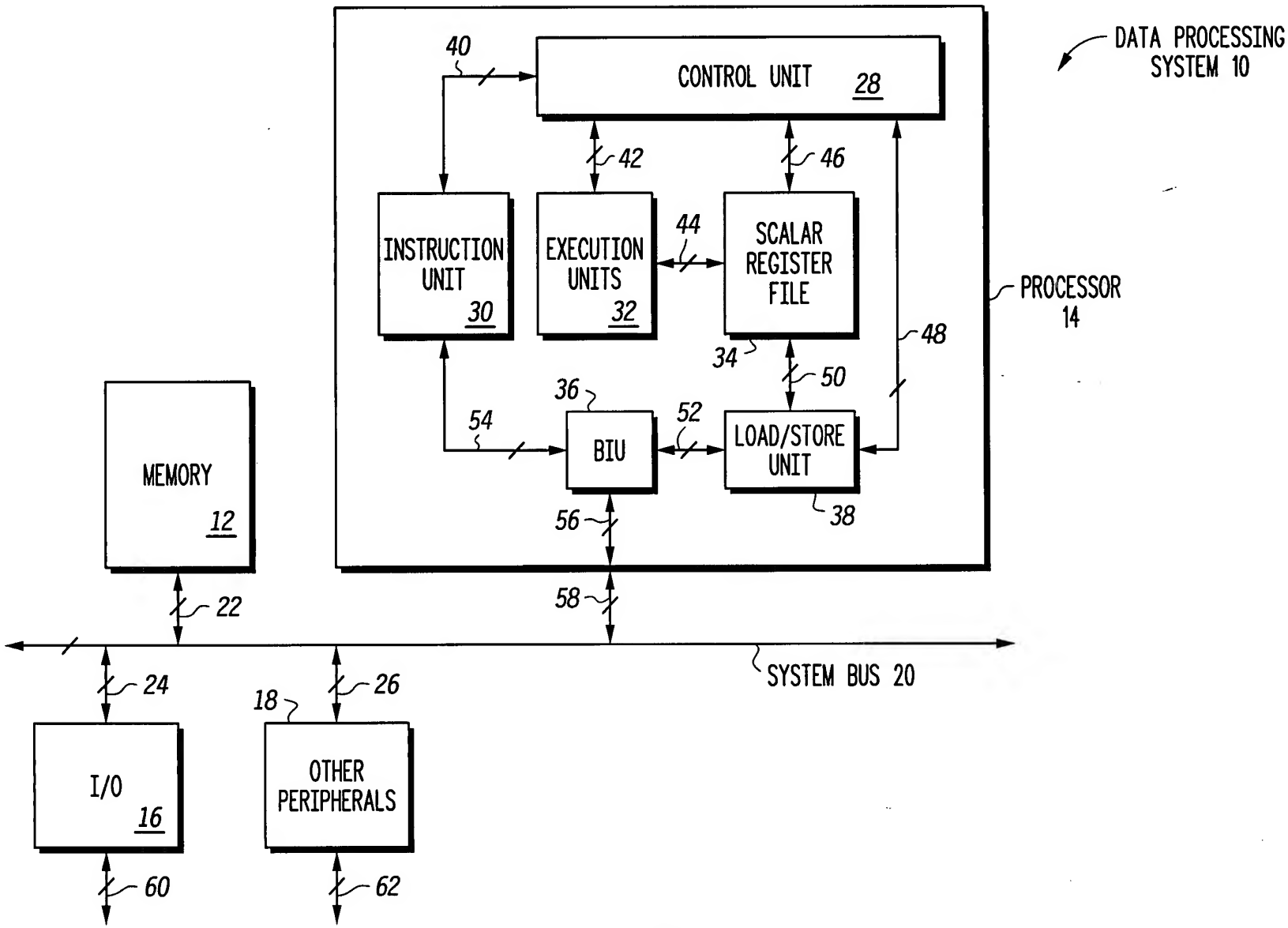

DATA PROCESSING SYSTEM 10
CONTROL UNIT 28
40
42
46
INSTRUCTION UNIT 30
EXECUTION UNITS 32
44
SCALAR REGISTER FILE
PROCESSOR 14
48
34
50
36
52
54
BIU
LOAD/STORE UNIT
38
56
MEMORY 12
22
58
SYSTEM BUS 20
24
26
18
I/O 16
OTHER PERIPHERALS
60
62

FIG. 1

lvex.[s/u].[ms].[ds] rD, rA, rB

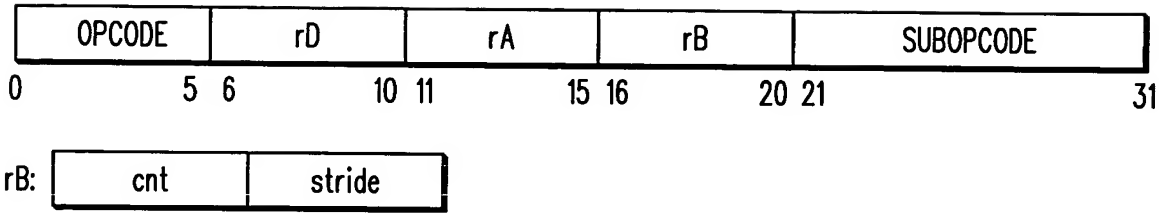


FIG. 2

lvex.[s/u].[ms].[ds] rD, rA, cnt, stride

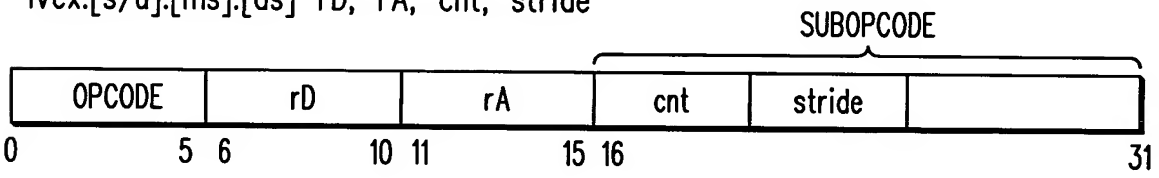


FIG. 3

lmvex.[s/u].[ms].[ds] rD, rA, rB

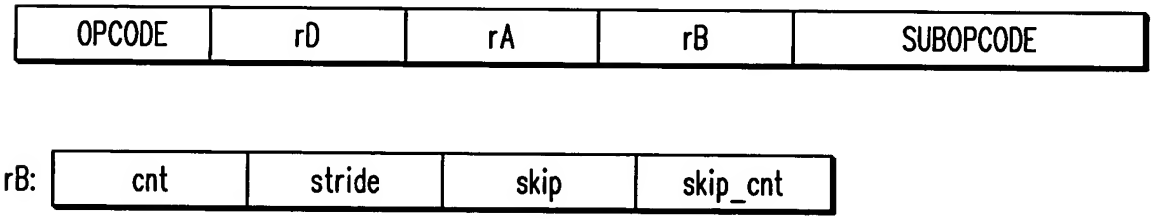


FIG. 4

lmvex.[s/u].[ms].[ds] rD, rA, cnt, stride, skip, skip_cnt

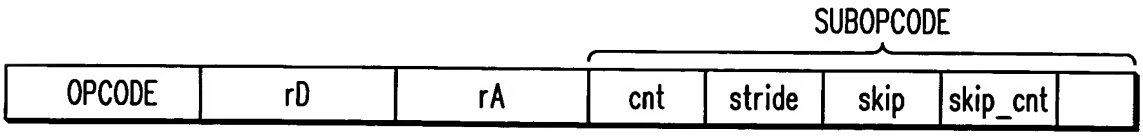


FIG. 5

lmvex2.[s/u].[ms].[ds] rD, rA, rB

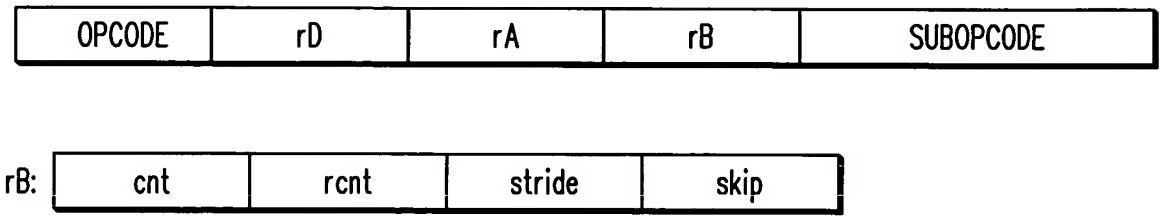


FIG. 6

lstrmvex.[s/u].[ms].[ds] rD, rA, rB

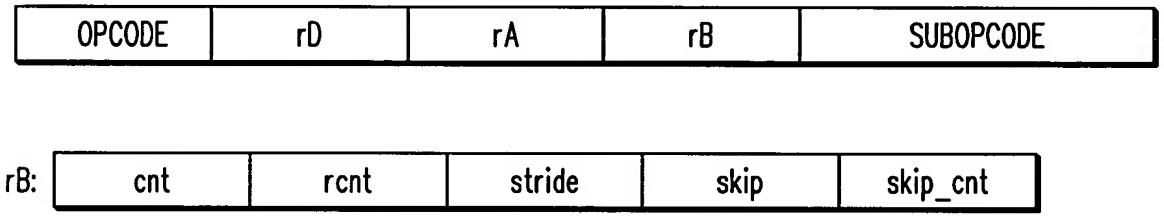


FIG. 7

stvex.[s/u].[ms].[ds].[h/l] rS, rA, rB

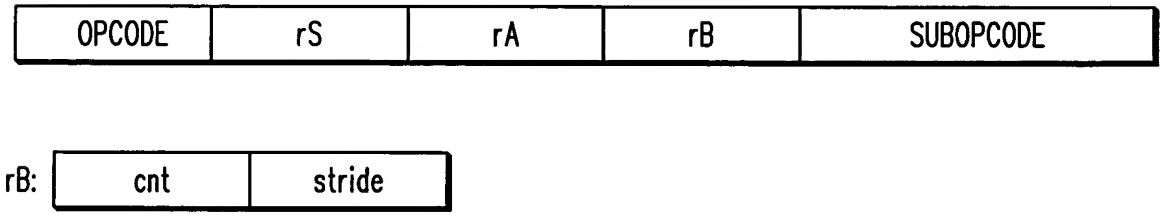


FIG. 8

stmvex.[s/u].[ms].[ss].[h/l] rS, rA, rB

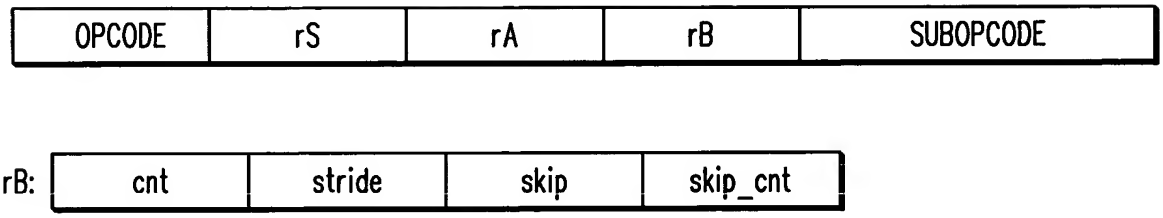


FIG. 9

stmvex2.[s/u].[ms].[ss].[h/l] rS, rA, rB

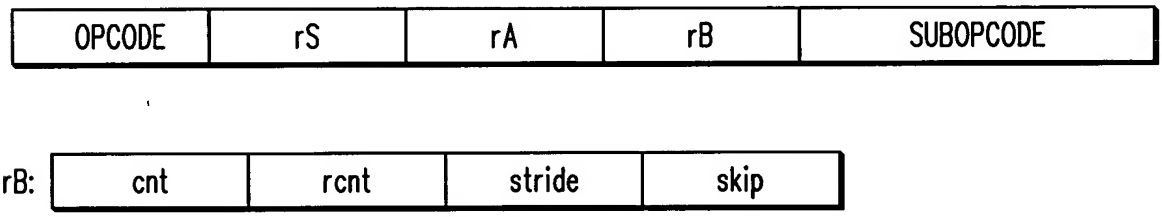


FIG. 10

ststrmvex.[s/u].[ms].[ss].[h/l] rS, rA, rB

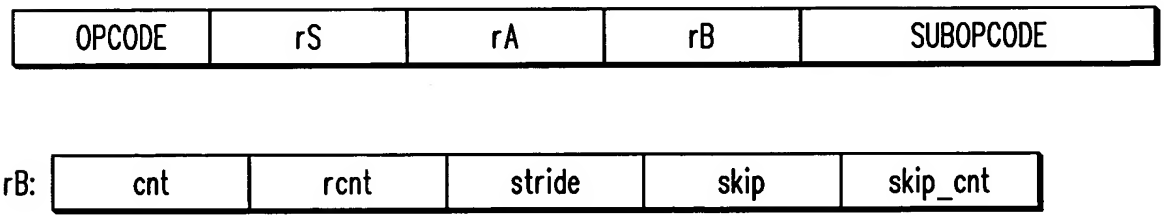


FIG. 11

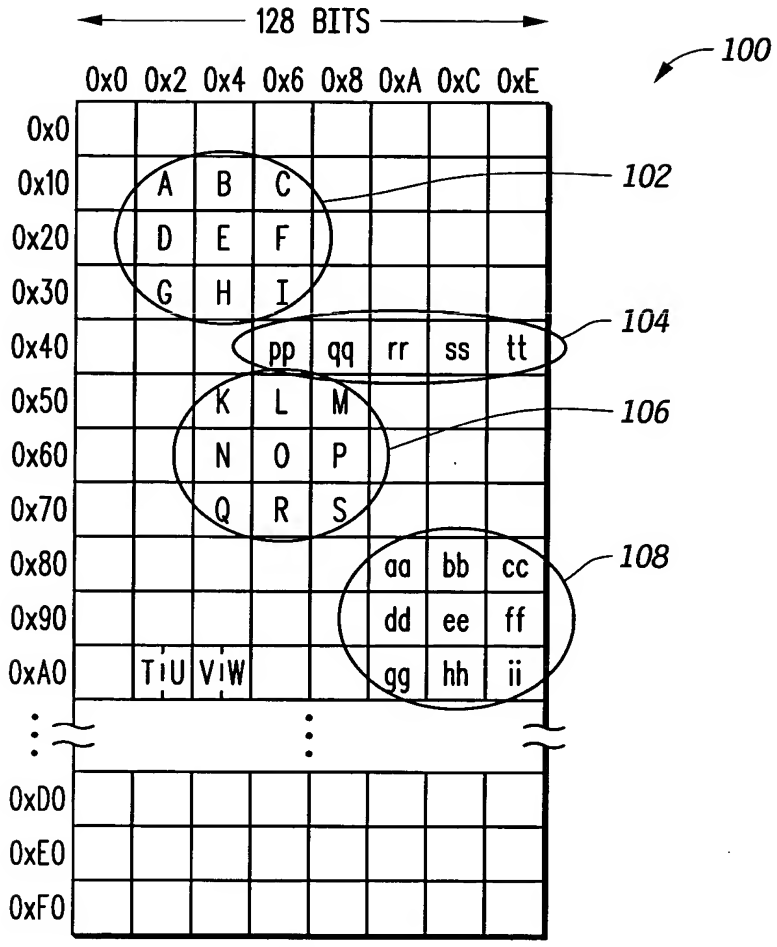


FIG. 12

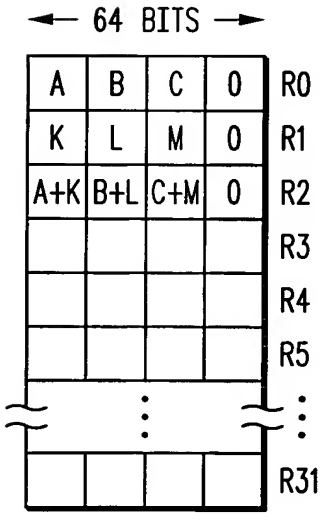


FIG. 13

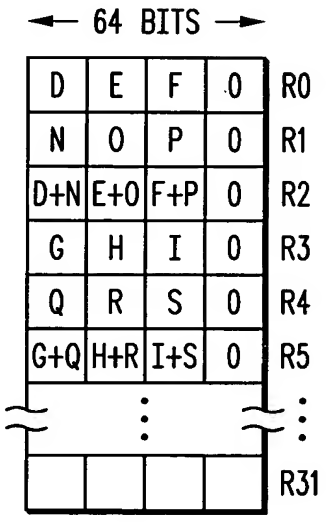


FIG. 14

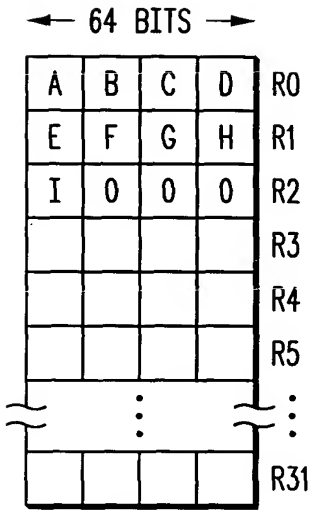


FIG. 15

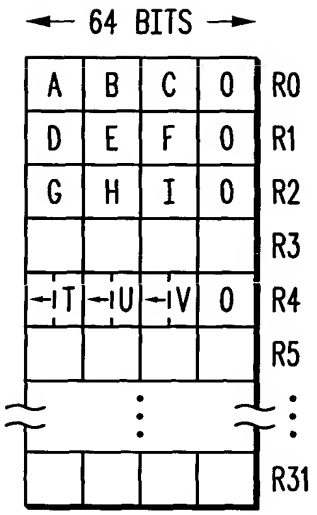


FIG. 16

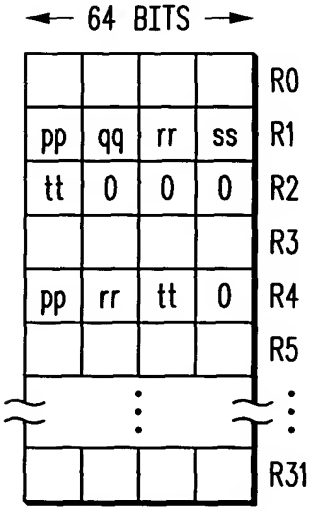


FIG. 17

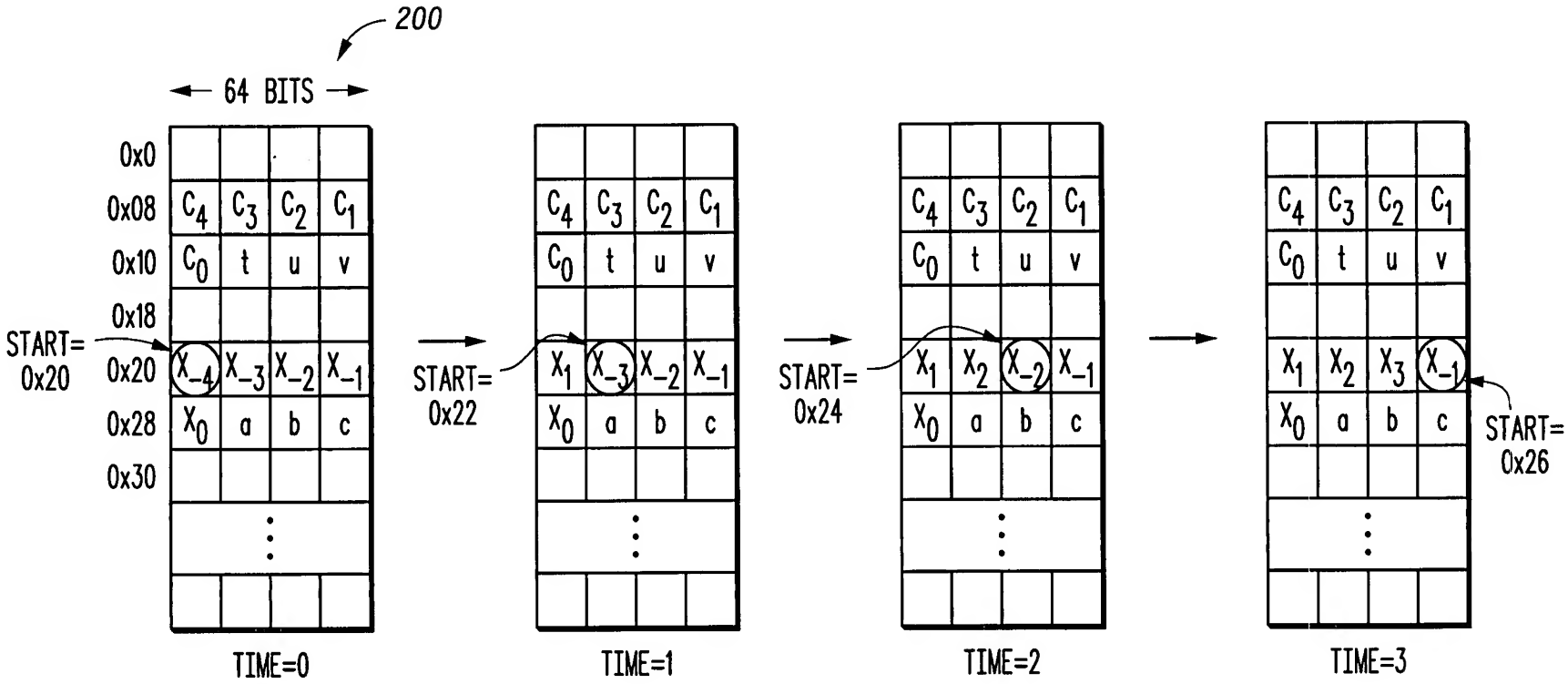

200
64 BITS
0x0
0x08
0x10
0x18
0x20
0x28
0x30
START=
0x20
START=
0x22
START=
0x24
START=
0x26
TIME=0
TIME=1
TIME=2
TIME=3

FIG. 18

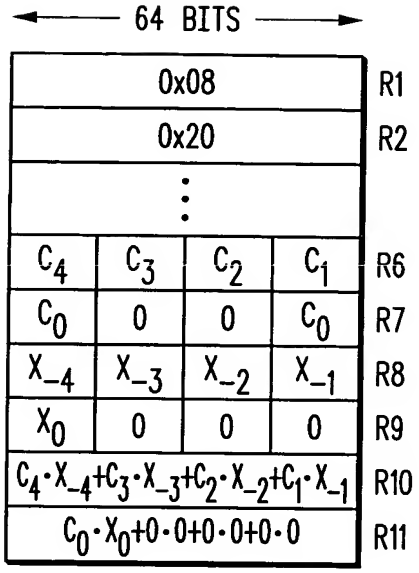


FIG. 19

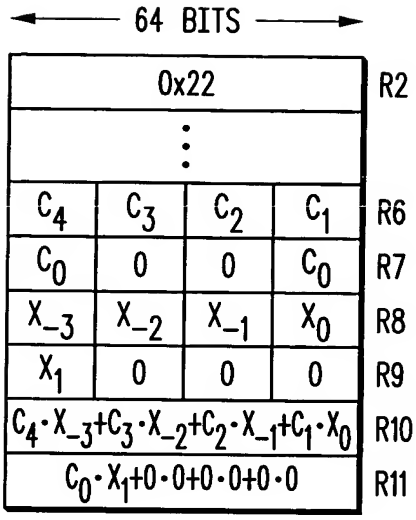


FIG. 20

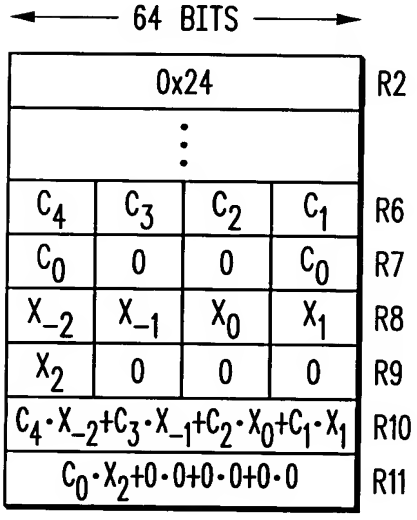


FIG. 21

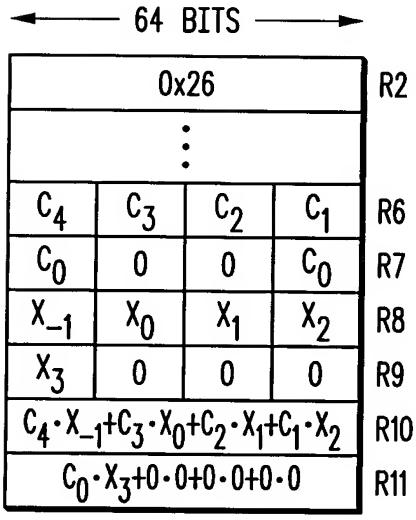


FIG. 22

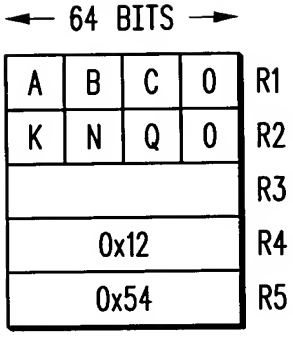


FIG. 23

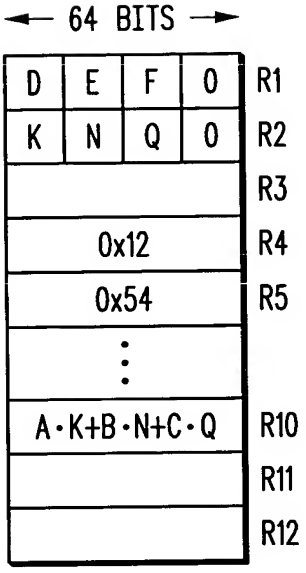


FIG. 24

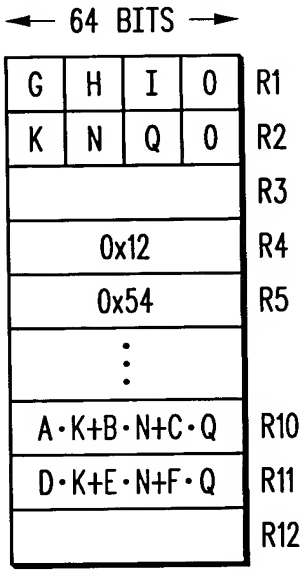


FIG. 25

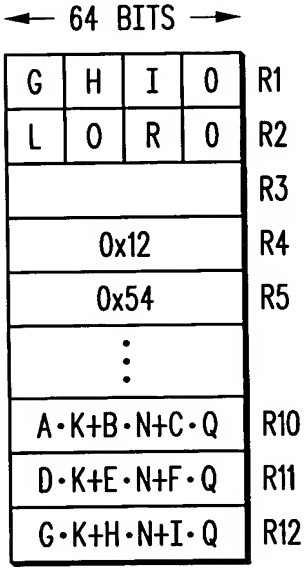


FIG. 26

lmvex_skip_once.[s/u].[ms].[ds] rD, rA, rB

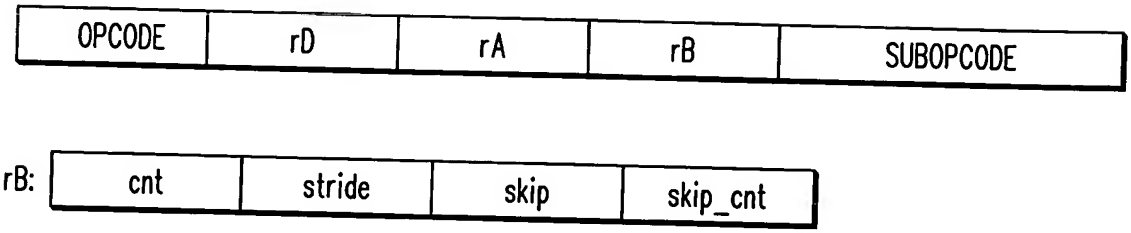


FIG. 27

lmvex_cb.[s/u].[ms].[ds] rD, rA, rB

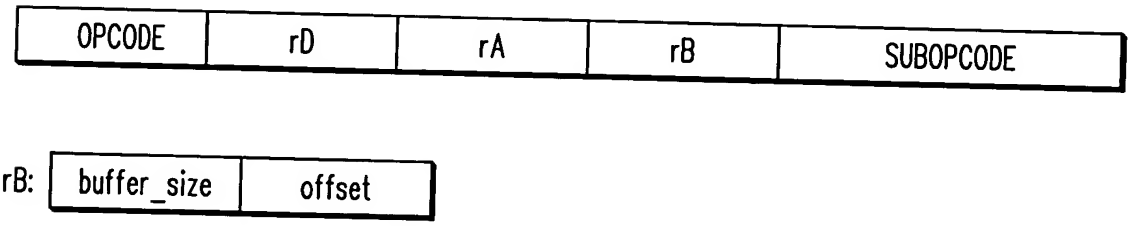


FIG. 28

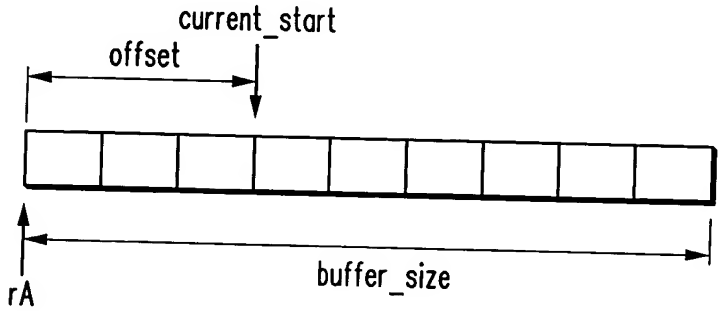


FIG. 29

lstrmvex_cb.[s/u].[ms].[ds] rD, rA, rB

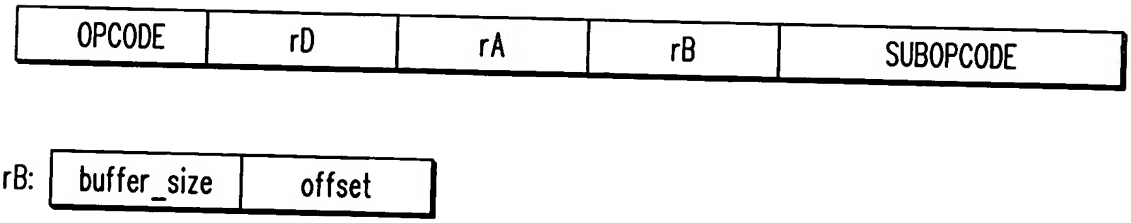


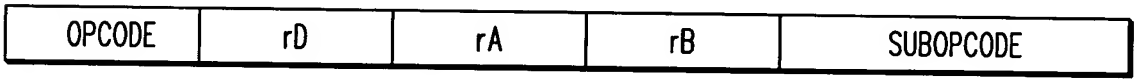
FIG. 30

lmvex_fft.[s/u].[ms].[ds] rD, rA, rB

rB: radix

FIG. 31

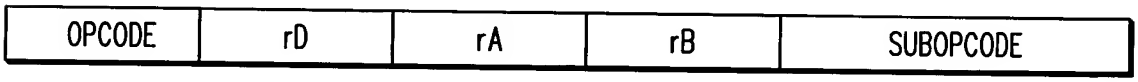
stmvex_fft.[s/u].[ms].[ss] rS, rA, rB



rB: radix

FIG. 32

lmstrmvex_fft.[s/u].[ms].[ds] rD, rA, rB



rB: radix

FIG. 33

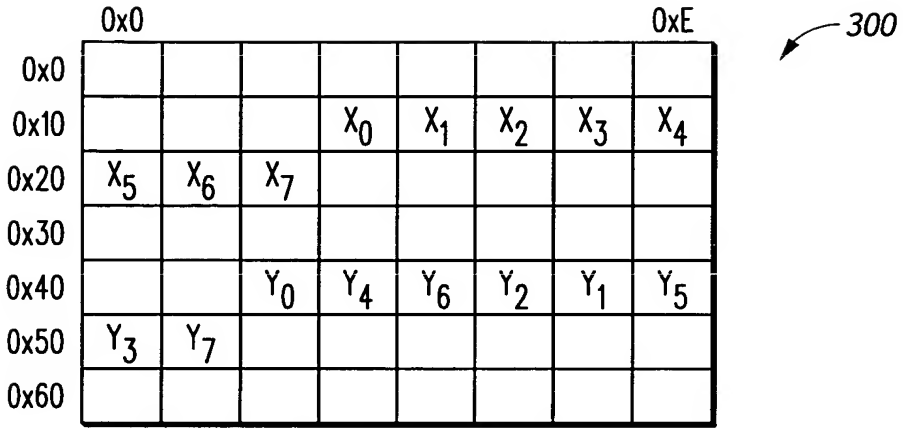


FIG. 34

X_0	X_4	X_6	X_2	R1
X_1	X_5	X_3	X_7	R2
				R3
Y_0	Y_1	Y_2	Y_3	R4
Y_4	Y_5	Y_6	Y_7	R5

FIG. 35